IN THE CLAIMS

Please cancel claims 9 and 10 and 13-16 without prejudice or disclaimer.

Please amend claims 1-8 and 11 as follows:

1. (Amended) An information processing system comprising:

a processor;

a memory; and

a memory controller connected with said processor via a first bus and connected with said memory via a second bus for controlling said memory,

said memory controller further comprising:

a buffer,

a control circuit,

an access judging circuit, wherein;

said control circuit estimates an most probable address to be accessed next in said memory,

said access judgement circuit prefetches a data stored in said most probable address of the memory into the buffer memory, before a memory access is carried out from said processor.

2. (Amended) An information processing system according to claim 1, wherein said memory controller comprises a direct path for transmitting data directly to said processor from said memory therethrough; said control circuit, when the access from said processor hits data within said buffer, is controlled to transfer the data to said processor, whereas, said control circuit, when the access from said processor fails to hit data within said

controlled to transfer data within said memory to said processor via said direct path.

3. (Amended) An information processing system according to claim 1, wherein said memory stores an instruction code to be executed on said processor therein, and said control circuit prefetches the instruction code into said buffer.

4. (Amended) An information processing system according to claim 1, wherein said memory stores therein an instruction code to be executed on said processor and operand data, and said control circuit prefetches the instruction code and operand data into said buffer.

5. (Amended) An information processing system according to claim 1, comprising a plurality of buffers into which data of said access unit is prefetched, and wherein said control circuit controls to transfer data already stored in said plurality of buffers to said processor in an order different from an address order.

6. (Amended) An information processing system according to claim 1, wherein said memory controller has an instruction decoder and a branching buffer, and said control circuit, when said instruction decoder detects a branch instruction, prefetches an instruction code as a branch destination into said branching buffer and, when an access is made from said processor to the instruction code, judges whether or not the instruction code hits data within said buffer and said branching buffer.

7. (Amended) An information processing system according to claim 1, wherein said memory controller has a register for instructing start or stop of the prefetch to said buffer.

8. (Amended) An information processing system according to claim 1, wherein said control circuit is controlled in its initial state to prefetch data already stored at a pre-specified address into said buffer.

11. (Amended) An information processing system according to claim 1, wherein said processor has an internal cache, and said control circuit is controlled to prefetch data having a data size of twice or more a line size of said internal cache into said buffer.